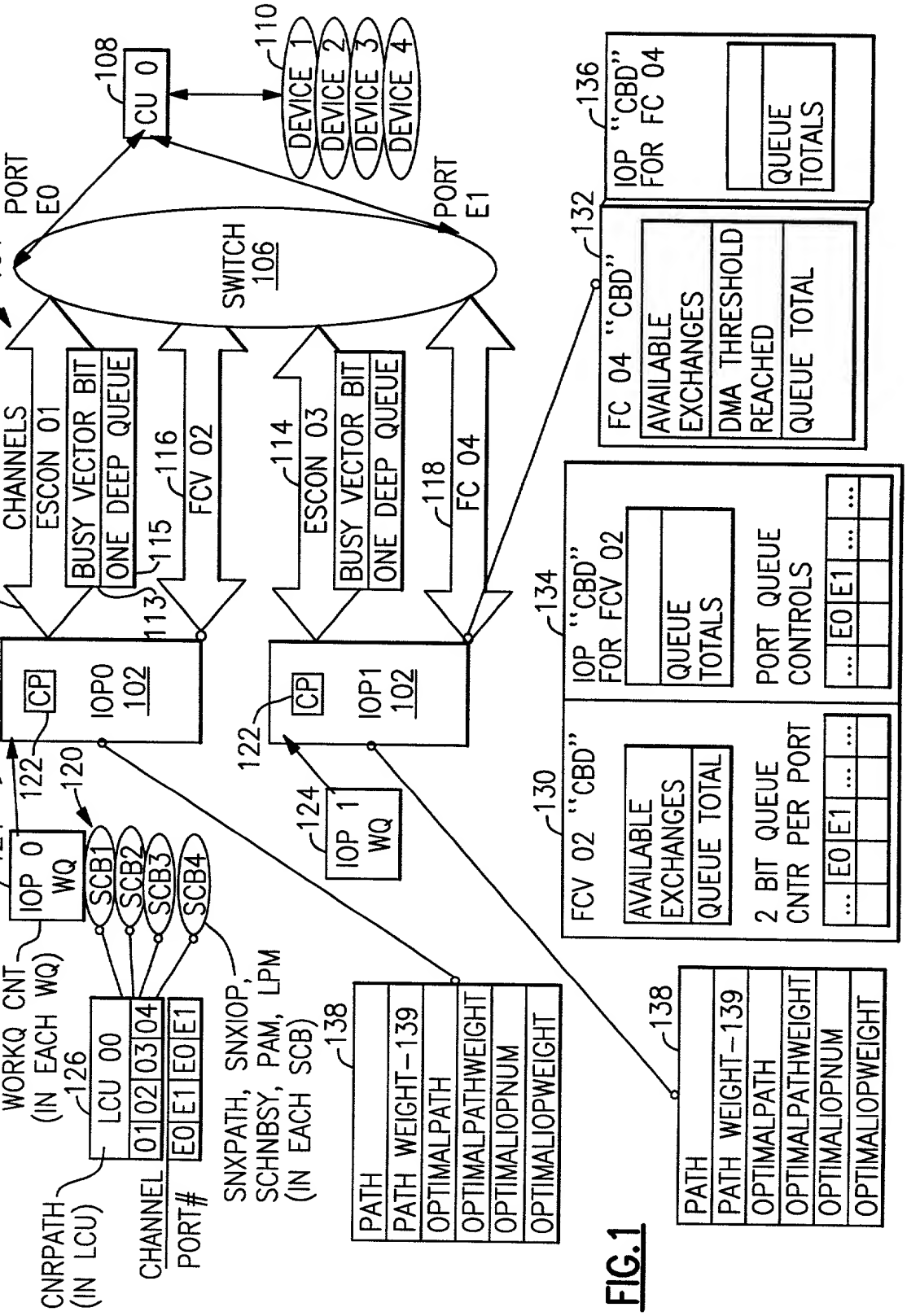
100
112
IOP0
102
CP
IOP1
102
CP
122
124
IOP 0
WQ
IOP 1
WQ
120
SCB1
SCB2
SCB3
SCB4
WORKQ CNT
(IN EACH WQ)
CNRPATH
(IN LCU)
LCU 00
01 02 03 04
E0 E1 E0 E1
CHANNEL
PORT#
SNXPATH, SNXIOP,
SCHNBSY, PAM, LPM
(IN EACH SCB)
CHANNELS
ESCON 01
BUSY VECTOR BIT
ONE DEEP QUEUE
115
116
FCV 02
113
ESCON 03
BUSY VECTOR BIT
ONE DEEP QUEUE
118
FC 04
104
PORT
E0
SWITCH
106
PORT
E1
108
CU 0
110
DEVICE 1
DEVICE 2
DEVICE 3
DEVICE 4
132
FC 04 "CBD"
AVAILABLE
EXCHANGES
DMA THRESHOLD
REACHED
QUEUE TOTAL
136
IOP "CBD"
FOR FC 04
QUEUE
TOTALS
134
IOP "CBD"
FOR FCV 02
QUEUE
TOTALS
PORT QUEUE
CONTROLS
... E0 E1 ... ...
130
FCV 02 "CBD"
AVAILABLE
EXCHANGES
QUEUE TOTAL
2 BIT QUEUE
CNTR PER PORT
... E0 E1 ... ...
138
PATH
PATH WEIGHT–139
OPTIMALPATH
OPTIMALPATHWEIGHT
OPTIMALIOPNUM
OPTIMALIOPWEIGHT
138
PATH
PATH WEIGHT–139
OPTIMALPATH
OPTIMALPATHWEIGHT
OPTIMALIOPNUM
OPTIMALIOPWEIGHT

FIG.1

130

| WORD OFFSET | BIT | DESCRIPTION | INITIAL SETTING BY IOP | VALUE STORED BY CHN |
|---|---|---|---|---|
| 0 | 0–7 | SEQUENCE NUMBER | 0 | SEQUENCE # |
| | 8–15 | AVAILABLE EXCHANGES | 0 | AVAILABLE LCs |
| | 16–31 | TOTAL QUEUED IN CHANNEL | 0 | TOTAL QUEUED |
| 1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER-WISE) | 0–7 | CONTROL BLOCK CODE | 0xFC | 0xFC |
| | 8 | CONTROL BLOCK CODE QUALIFIER | 0 | 0 |
| | 9–12 | RESERVED | 0 | 0 |
| | 13 | CHN UNAVAILABLE (NOT USED) | 0 | 0 |
| | 14 | CHN ALLOWED TO STORE INTO AREA | 1 | 1 |
| | 15 | CHN DID STORE INTO AREA | 0 | 1 |
| | 16–23 | CHID | CHID | CHID |
| | 24–31 | RESERVED | 0 | 0 |
| 2–17 | 2x256 | 2 BITS PER PORT QUEUE COUNTERS | 0 | SET PER PORT |
| 18–31 | | RESERVED – FOR EITHER CHN OR IOP (JUST IN CASE) | 0 | DON'T STORE ANYTHING |

FIG.2

132

| WORD OFFSET | BIT | DESCRIPTION | INITIAL SETTING BY IOP | VALUE STORED BY CHN |
|---|---|---|---|---|
| 0 | 0–7 | SEQUENCE NUMBER | 0 | SEQUENCE # |
| | 8–15 | AVAILABLE EXCHANGES | 0 | AVAILABLE EXCH. |
| | 16–31 | TOTAL QUEUED IN CHANNEL | 0 | TOTAL QUEUED |
| 1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER-WISE) | 0–7 | CONTROL BLOCK CODE | 0xFC | 0xFC |
| | 8 | CONTROL BLOCK CODE QUALIFIER | 0 | 0 |
| | 9–12 | RESERVED | 0 | 0 |
| | 13 | CHN UNAVAILABLE (NOT USED) | 0 | 0 |
| | 14 | CHN ALLOWED TO STORE INTO AREA | 1 | 1 |
| | 15 | CHN DID STORE INTO AREA | 0 | 1 |
| | 16–23 | CHID | CHID | CHID |
| | 24 | DMA STORAGE REQUEST QUEUE THRESHOLD REACHED | 0 | SET TO 1 IF REACHED |
| | 25–31 | RESERVED | 0 | 0 |
| 2–31 | | RESERVED – FOR EITHER CHN OR IOP (JUST IN CASE) | 0 | DON'T STORE ANYTHING |

FIG.3

134

| WORD OFFSET | BIT | DESCRIPTION | INITIAL SETTING BY IOP | VALUE STORED BY IOP |
|---|---|---|---|---|
| 0 | 0–7 | SEQUENCE NUMBER | 0 | SEQUENCE # |
| | 8–15 | RESERVED | 0 | 0 |
| | 16–31 | TOTAL QUEUED IN CHANNEL | 0 | TOTAL QUEUED |
| 1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER-WISE) | 0–7 | CONTROL BLOCK CODE | 0xFC | 0xFC |
| | 8 | RESERVED | 1 | 1 |
| | 9–13 | | 0 | 0 |
| | 14 | IOP ALLOWED TO STORE INTO AREA | 1 | 1 |
| | 15 | IOP DID STORE INTO AREA | 0 | 1 |
| | 16–23 | CHID | CHID | CHID |
| | 24–31 | RESERVED | 0 | 0 |
| 2–9 | 1x256 | IOP_Q2BUSY | 0 | SET PER PORT |
| 10–17 | 1x256 | IOP_Q1BUSY | 0 | SET PER PORT |
| 18–25 | 1x256 | IOP_PREVQBUSY | 0 | SET PER PORT |
| 26–31 | | RESERVED | 0 | 0 |

FIG.4

136

| WORD OFFSET | BIT | DESCRIPTION | INITIAL SETTING BY IOP | VALUE STORED BY IOP |
|---|---|---|---|---|
| 0 | 0–7 | SEQUENCE NUMBER | 0 | SEQUENCE # |
| | 8–15 | RESERVED | 0 | 0 |
| | 16–31 | TOTAL QUEUED IN CHANNEL | 0 | TOTAL QUEUED |
| 1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER-WISE) | 0–7 | CONTROL BLOCK CODE | 0xFC | 0xFC |
| | 8 | CONTROL BLOCK CODE QUALIFIER | 1 | 1 |
| | 9–13 | RESERVED | 0 | 0 |
| | 14 | IOP ALLOWED TO STORE INTO AREA | 1 | 1 |
| | 15 | IOP DID STORE INTO AREA | 0 | 1 |
| | 16–23 | CHID | CHID | CHID |
| | 24–31 | RESERVED | 0 | 0 |
| 2–31 | | RESERVED | 0 | 0 |

FIG.5

139

| BIT | DESCRIPTION | FCV | FC | NON-FICON |
|---|---|---|---|---|
| 0-1 | NUMBER OF STARTS QUEUED TO PORT -OR- BUSYNESS OF CHANNEL | CHN_QCOUNT(PORT) + IOP_Q1BUSY(PORT) + IOP_Q2BUSY(PORT) (TOTAL NUMBER OF STARTS QUEUED TO THE PORT) | 0 | 0 |
| 2 | | | FC__UMAXSTOREREQS + "AEX" NOTE: TO COMPUTE AEX: IF AVAILABLEEXCHANGES = 0, THEN "AEX" = 1. OTHERWISE, "AEX" = 0 | ONE DEEP QUEUE BIT FROM VECTOR. FOR PRE-zSERIES, SET BIT TO 0 |
| 3 | | | | CHANNEL BUSY VECTOR BIT |
| 4 | LINK INIT REQ'D | IF LINK INIT REQUIRED, SET BIT TO 1 | | |
| 5 | PREVIOUSLY QUEUED START | IOP_PREVQBUSY(PORT) | 0 | 0 |
| 6 | DESTINATION PORT BUSY | 0 | 0 | 0 |
| 7 | CHANNEL HARDWARE AVAILABILITY | IF AVAILABLEEXCHANGES = 0, SET BIT TO 1. OTHERWISE, SET TO 0 | "AEX" -OR'D WITH - FC__MAXSTOREREQS | CHANNEL BUSY VECTOR BIT |
| 8-13 | RESERVED | 0 | 0 | 0 |
| 14 | UNKNOWN PATHWEIGHT STATE | IF FICON PATH NOT STORING STATISTICS IN HSA (FC/FCV_STATSACTIVE = 0), SET THIS BIT TO 1. FOR PRE-zSERIES NON-FICON PATHS: IF PATH IS ON ANOTHER IOP -OR- THE CHANNEL BUSY VECTOR IS ON, SET THIS BIT TO 1 | | |
| 15 | FAVOR PREFERRED PATH | SET TO 1 IF PREFERRED PATH BIT IS ON & THIS PATH IS NOT PREFERRED PATH | | |
| 16-31 | TOTAL QUEUED IN CHANNEL | FCV_TOTALQUEUED + IOP_TOTALQUEUED | FC__TOTALQUEUED + IOP_TOTALQUEUED | CHANNEL BUSY VECTOR BIT x 8 |

FIG.6